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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/812,346	OGATA, YOSHIHARU	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-6,8-12 and 21-25* is/are pending in the application.

4a) Of the above claim(s) *3, 8-10 and 12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-6,11 and 21-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1, 4, 6, 11, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US Pat. Application Pub. 2002/0096754) in view of Fogal et al. (US Pat. 5323060) and Eguchi et al. (US Pat. 6784541).

Regarding claims 1, 4, 21 and 22, Chen et al. disclose a semiconductor device (Fig. 2) comprising:

- a substrate provided with terminals (22 and 26 respectively in Fig. 2) for connecting conductive wires
- a first semiconductor chip/integrated circuit (IC) mounted face-up on the substrate and electrically connected to the terminals provided on the substrate by the conductive wires (see 34 and 44 respectively in Fig. 2), and
- a second semiconductor chip/IC having recesses and a projecting part (see 46/51 in Fig. 2) formed on a rear surface thereof and attached onto the first semiconductor chip via the projecting part, and

- an adhesive that attaches the second semiconductor chip/IC onto the first semiconductor chip/IC via the projecting part and fills regions of the recessed/stepped part of the projecting part (see 52 in Fig. 2)

(Fig. 2, sections 0020-0025).

Chen et al. fail to teach:

a) an insulating resin being used as the adhesive for the attachment, and

b) an insulating layer formed on an entire rear surface of the second semiconductor chip including the projecting part so as to be interposed between the first and second chips.

a) Fogal et al. teach using an adhesive comprising a conventional insulating material such as an epoxy paste/resin or a tape/sheet for an attachment of a second chip with a first chip (see 38 in Fig. 1; Col. 2, lines 49- Col. 3, line 11).

b) Eguchi et al. teach a device (see Fig. 7C-7H) wherein an insulating resin/layer (see 7 in Fig. 7C) is formed on an entire surface/rear surface opposing the surface having connection pads to provide the desired adhesion and thermal dissipation (Col. 11 lines 1-16).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the elements a) and b) as taught by Fogal et al. and Eguchi et al. so that the desired insulation, adhesion and protection for the chips and

the bonding wires can be achieved and reliability can be improved in Chen et al's device.

Regarding claim 6, Chen et al., Fogal et al. and Eguchi et al. teach the entire claimed structure as applied to claim 1 above, wherein Chen et al. further teach:

- first bonding/electrode pads (42 in Fig. 2) provided on the first semiconductor chip/IC
- first conductive wires (44 in Fig. 2) electrically connecting the first electrode pads to the terminals provided on the substrate
- second bonding/electrode pads (42 in Fig. 2) provided on the second semiconductor chip/IC, and
- second conductive wires (44 in Fig. 2) electrically connecting the second bonding/electrode pads and the terminals provided on the substrate, and
- the adhesive (50 in Fig. 2) provided between the first semiconductor chip/IC and the second semiconductor chip/IC so as to be present below the second bonding/electrode pads and attaching the second semiconductor chip/IC onto the first semiconductor chip/IC via the projecting part.

Regarding claim 11, Chen et al., Fogal et al. and Eguchi et al. teach the entire claimed structure as applied to claim 1 above, wherein Chen et al. teach the device comprising

the first and the second semiconductor chips/IC/electronic components (Fig. 2, sections 0020-0025).

3. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US Pat. Application Pub. 2002/0096754) in view of Fogal et al. (US Pat. 5323060), Eguchi et al. (US Pat. 6784541) and LoBianco et al. (US Pat. 6340846).

Regarding claim 5, Chen et al., Fogal et al. and Eguchi et al. teach the entire claimed structure as applied to claim 1 above, wherein Chen et al. further teach:

- first bonding/electrode pads (42 in Fig. 2) provided on the first semiconductor chip/IC
- first conductive wires (44 in Fig. 2) electrically connecting the first electrode pads to the terminals provided on the substrate
- second bonding/electrode pads (42 in Fig. 2) provided on the second semiconductor chip/IC, and
- second conductive wires (44 in Fig. 2) electrically connecting the second bonding/electrode pads and the terminals provided on the substrate

Chen et al., Fogal et al. and Eguchi et al. fail to teach a sealing resin sealing the first semiconductor chip to which the first conductive wires are connected and the second semiconductor chip to which the second conductive wires are connected.

LoBianco et al. teach a stacked device (see Fig. 6) wherein an insulating adhesive/encapsulate resin (see 64/60 in Fig. 6) is formed to seal the first and the second semiconductor chips/IC and respective wires (see 14, 16, 38 and 64/60 in Fig. 6; Col. 5).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the sealing resin sealing the first semiconductor chip to which the first conductive wires are connected and the second semiconductor chip to which the second conductive wires are connected as taught by LoBianco et al. so that the desired protection for the chips and the bonding wires can be achieved in Eguchi et al., Fogal et al. and Chen et al's device.

4. Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US Pat. Application Pub. 2002/0096754), Fogal et al. (US Pat. 5323060) and Eguchi et al. (US Pat. 6784541) as applied to claim 1 above, and further in view of Taar et al. (US Pat. Application Pub. 2004/0026768).

Regarding claims 23 and 24, Chen et al., Fogal et al. and Eguchi et al. teach the entire claimed structure as applied to claim 1 above, except the thickness of the second semiconductor chip being approximately 50-200 microns or that of projecting part being approximately 30-150 microns.

Taar et al. teach a stacked/multichip package using chips/dice having thickness in a range of approximately 120-240 microns (5-10 mils) and that of projecting part being

approximately 100-150 microns/4-6 mils (see 140/240 in Fig. 1A/2A; sections 0026-0031).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the thickness of the second semiconductor chip being approximately 50-200 microns or that of projecting part being approximately 30-150 microns as taught by Taar et al. so that the desired package dimensions, wafer/chip process yield and wire bonding reliability can be achieved surface protection and thermal dissipation can be improved in Eguchi et al., Fogal et al. and Chen et al's device.

5. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US Pat. Application Pub. 2002/0096754), Fogal et al. (US Pat. 5323060) and Eguchi et al. (US Pat. 6784541) as applied to claim 1 above, and further in view of Connell et al. (US Pat. Appl. Pub. 2003/0162368).

Regarding claim 25, Chen et al., Fogal et al. and Eguchi et al. teach the entire claimed structure as applied to claim 1 above, except the insulating layer comprising a silicon oxide film or a silicon nitride film.

Connell et al. teach wafers/chips with entire backside having a film/layer (50 in Fig. 12) comprising a variety of materials including silicon oxide, silicon nitride film or tape/polymeric to provide stress reduction and improved adhesion and surface protection (see sections 0017-0019, 0060-0062, 0071, 0075 and pp. 3-6).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the insulating layer on the entire rear surface of the second chip comprising a silicon oxide film or a silicon nitride film as taught by Connell et al. so that the desired adhesion, surface protection can be achieved and reliability can be improved in Eguchi et al., Fogal et al. and Chen et al's device.

Response to Arguments

6. Applicant's arguments filed on 01-17-06 have been fully considered but they are not persuasive.

A. Applicant contends that Eguchi is not directed to stacked chips and fails to disclose an insulating layer formed on an entire rear surface of the second semiconductor chip including the projecting part that extends below the second semiconductor chip so as to be interposed between the first and second chips.

However, as explained in the rejections above, Eguchi et al. is applied to the second chip in Chen et al's stacked device to provide the insulating layer on the entire rear surface of the chip as taught in the chip structure (see layer 7 on the chip 1 in Fig. 7C) in Eguchi et al's resin bonded device to provide the desired adhesion and thermal dissipation. The primary reference of Chen et al. discloses the stacked chip device and the second chip having projecting part on the rear surface as claimed.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAN or Public PAG. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAG system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

NP

03-15-06

NITIN PAREKH

PRIMARY EXAMINER

TECHNOLOGY CENTER 2800